AN INNOVATIVE OPEN-LOOP CDR BASED ON INJECTION-LOCKED OSCILLATOR FOR HIGH-SPEED DATA LINK APPLICATIONS

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ABSTRACT

A new fully integrated clock and data recovery (CDR) architecture based on an injection-locked oscillator is presented in this paper. Two circuits, implemented in CMOS VLSI technology and dedicated to 1 Gbps point-to-point networks, will be detailed. This open-loop CDR topology is compared with classical ones (high-Q filter, phase-locking, ...) in term of power consumption, silicon area and complexity. Our circuits exhibit some major advantages versus traditional CDRs: no external component needed, low consumption and low locking time. It is a very simple way to achieve clock extraction and data regeneration for high-speed data link applications.

I. INTRODUCTION

The design of the clock and data recovery (CDR) circuit is the most challenging part of building a high-speed receiver because of the complexity of this unit. In this block, a clock signal is generated such that its rising and/or falling edges fall in the middle of the data eye. This means that if the clock signal is used to retime the data, the sampling occurs at the optimum point, improving the SNR of the receiver.

In the second section, we will discuss on the different architectures conventionally used in CDR systems, comparing their advantages and drawbacks, in term of complexity, locking time, power dissipation and cost.

While most of the classical CDRs used and published in the literature are based on phase-locking architecture, we present in the third section a novel approach based on an open-loop topology using an injection-locked oscillator, in order to realize low cost, high performance and low power consumption system. Moreover, it takes advantage of a simple structure, leading a significant time-to-market reduction.

We describe in the fourth paragraph the theoretical approach and the circuit architecture to design such a topology for high-speed data link and the measurement results of circuit dedicated to 1 Gbps point-to-point networks are presented in the last section.

II. PRINCIPLE OF CLOCK AND DATA RECOVERY

A clock and data recovery circuit is a key component for optical transmission receivers. It consists of a clock recovery circuit for realizing retiming and a decision circuit for achieving regeneration. Researches on CDR are emphasizing due to the operating speed increase as well as for fully monolithic integration, for optimization in term of size, cost and reliability.

CDR circuits can be categorized into two main groups: open-loop (or filter-based) CDRs [1] with high-Q filter or injection-locked oscillator [2], and CDRs employing phase-locked loops (PLL) [3] or delay-locked loop (DLL) [4] with bang-bang or linear phase detector.

The closed-loop configurations consist in synchronizing the incoming data with an oscillator.

If the latter is controlled by a voltage (VCO), it is a Phase-Locked Loop based configuration. When the oscillator is build on a chain of logic gates with programmable delay (voltage controlled delay line), then it is called Delay-Locked Loop architecture. A major advantage of these structures is that the recovered clock is automatically aligned with input data. The decision circuit is then relaxed in term of complexity.

Nevertheless, the design of such systems suffers from high complexity in high-speed data links, mainly through the realization of the phase or phase-frequency detector. Due to the major blocks running at the bit clock, the power consumption is usually high.

Concerning the PLL-based structure, minimizing jitter due to power supply noise requires maximizing loop bandwidth. Unfortunately, arbitrarily large loop bandwidth is not possible because all practical feedback systems suffer of phase margin degradation. In conjunction with the need to absorb component tolerances and drifts with temperature and power supply force the use of loop bandwidths that are only a small fraction (less than 10%) of the clock frequency to guarantee acceptable worst-case phase margins.

Therefore, because the loop bandwidth is often much smaller than the tuning range, acquisition is generally slow, even with frequency-acquisition aids. Indeed, the large value of the filter capacitor usually imposes an external component –which is source of extra noise. This problem can be eliminated by integrating the capacitor, as the matter of consequence increasing in the same way the amount of silicon area.

Using a DLL configuration, only phase acquisition needs to take place: acquisition can then be faster than that of PLL's. And, unlike the case of a PLL, jitter filtering is independent of the loop bandwidth, so that only acquisition speed and loop stability considerations bound the loop bandwidth.

In conventional clock and data recovery circuit using a nonlinear clock extraction technique, a clock signal is

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extracted from the input data by differentiating and rectifying circuits. In order to maintain the clock signal during consecutive input '1' or '0', a high-Q filter and a high-gain limiting amplifier are used. The input data is retimed in the decision circuit, where a tunable delay generator is used to precisely adjust the clock timing.

The major advantages of these structures are the simple architecture, the low power consumption and the low silicon area used. Nevertheless, off-chip components (resonator, SAW, ...) are mandatory to provide high selectivity in the filtering process.

III. Proposed Architecture

In this paper, we propose an innovative solution to deal with the previous problems in term of power consumption, die area, external component and acquisition time [5]. In the open-loop configuration, we take advantage of the injection-locked oscillator (also called Synchronous Oscillator SO) usually used in RF synthesizers [6], and we have adapted the theory to the clock regeneration.

Fig. 1 depicts the block diagram of the CDR circuit. As conventional ones, two building blocks are implemented: one for the clock recovery and the second for the data recovery and synchronization versus the clock.

The clock recovery is based on the use of a Synchronous Oscillator, built with a classical oscillator associated with a pulse generator. The principle of operation [6] is to stimulate an oscillator by an input signal where the input frequency is closed to the free running one. Then the oscillator will lock on this input reference. The pulse generator block is implemented in order to create sharp edges at the input of the oscillator to smooth the progress of synchronization.

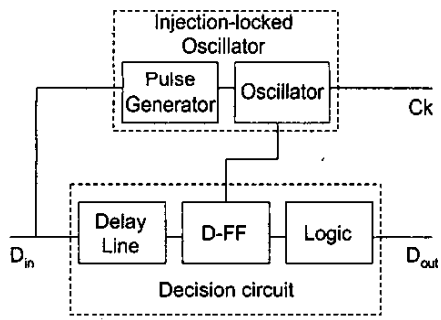

Figure 1. Block diagram of the open-loop CDR

When no data is delivered to the input data lines, the output clock is given by the free running frequency of the oscillator. When the bits flow is set the SO is synchronized on the input data rate. The bit clock is then recovered.

Unlike RF applications where the carrier is a continuous waveform, the input reference is a pseudo-random signal. Indeed, the pulse generator does not deliver a periodic pulse but also a pseudo-random one. The oscillator is then synchronized by multiple harmonics of the input signal. All these transitions resynchronize the oscillator, so the average frequency is the same than the data rate.

This proposed CDR is categorized as a nonlinear clock extraction circuit, while the injection-locking principle is used. This is because the nonlinear clock frequency component extraction process is common to both the proposed CDR and the conventional nonlinear one, which consists of a differentiater, rectifier, limiting amplifier and high-Q filter. The difference between them is the circuit configuration realizing the filtering function and amplification. In the proposed CDR, the SO realizes these functions simultaneously.

IV. Circuit Configuration

The synchronous oscillator, as shown in Fig. 2, uses a negative resistance configuration. The PMOS transistor P_1 keeps the voltage headroom with regards to the positive supply rail for the synchronization network to act properly. The integrated inductors are based on metal4-metal5 structure. In order to perform differential operation, the capacitor C is split into two identical ones, chosen to optimize the locking range. The free running frequency is targeted to 1.1 GHz.

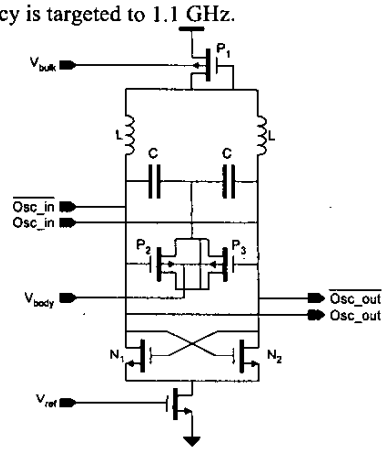

Figure 2. Negative resistance oscillator

In order to be robust versus process variations, two additional circuits have been added, based on the body effect of PMOS transistors P_1-P_3. It allows us the control of the free running frequency of the oscillator. Due to the large synchronization range, this control system could be coarse, and then operated automatically through a straightforward DAC. The frequency deviation obtained is 100 MHz.

The synchronization network (pulse generator) is depicted in Fig. 3.

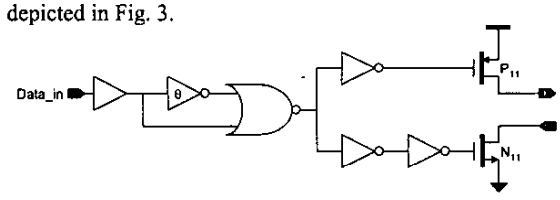

Figure 3. Pulse generator schematic

The synchronization range is done by equation 1.

$$\Delta f = \frac{I_0}{(\pi)^2 \sqrt{2} \cdot V_s \cdot C_{equ}} \quad (1)$$

with I_0 the current pulse amplitude of the synchronization network, V_s the output peak-to-peak amplitude and C_{equ} the equivalent capacitance of the LC-tank.

P_{11} and N_{11} drains are directly shorted to the output of the oscillator in Fig. 2 to fulfill the SO. In order to synchronize the oscillator on the input data rate, this block has to generate a current pulse, which duration equal to half the period of the wanted frequency [6].

Two prototypes have been integrated [7] in order to evaluate the impact of the synchronization range on the clock jitter. They provide respectively 5 and 9 mA differential-like pulses between its outputs at each rising edge of the synchronization clock, which leads to about 200 and 600 MHz of synchronization range. This is large enough to cover process variations, according to our free-running frequency control.

The decision circuit objective is to synchronize the data frame with the internal recovered clock. Fig. 4 shows a circuit diagram of the decision circuit based on a voting sequence. It consists of a comparison between few D Flip-Flops.

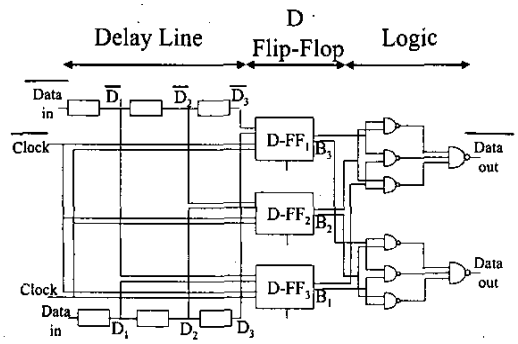

Figure 4. Decision circuit diagram

The data frame goes through two delay lines. Each line is built with three delay elements, which generate three identical delays D_1, D_2 and D_3. The delay is chosen so that D_2 frame is synchronized with the falling edge of the clock. In this application, the frequency is 1 GHz, so each delay element is optimized at 250 ps. D_3 is then 750 ps behind the rising edge of the clock. Therefore, two of three delayed lines will always be in a bit period. The six lines are synchronized with the clock into three D Flip-Flops, D-FF_1, D-FF_2, and D-FF_3.

The data frame is synchronized on the falling edge of the clock. For this reason, another D Flip-Flop, added at the output of the decision circuit, will synchronize the data on the rising edge of the recovered clock.

The decision circuit includes 50 Ω output buffers in order to drive the classical instrumentation.

V. MEASUREMENTS

Fig. 5 depicts the chip microphotograph of the clock and data recovery. The process used is a low cost CMOS VLSI 0.18µm from STMicroelectronics. The area of the core is roughly 0.7 mm². Due to the parasitic components yielded by the package, a large number of power bondings were used in addition with on-chip decoupling capacitors. Indeed, the vacant part of the die (4 mm²) is filled with large decoupling capacitors (450 pF). This circuit demonstrates than the synchronous oscillator can be used as clock recovery without any external component.

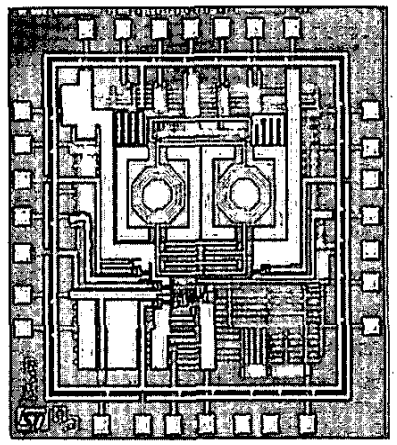

Figure 5. Chip microphotograph

The current consumption is roughly 40 mA under 1.8 V supply voltage (excluding the four 50 Ω output buffers).

The free running frequency of the clock recovery is 1.09 GHz and the synchronization range is around 190 and 600 MHz, in good agreement with the theory, depending of the synchronization range. The generated clock exhibits, at 200 kHz from the carrier, a phase noise equal to –119 dBc/Hz.

When a recurring bit pattern is applied at 1 Gbps, the rms measured jitter is 1.6 ps (Fig. 6). In fact, this jitter is only representative of Anritsu 1632A generator random noise, which is 1.3 ps rms. It confirms that the synchronization process leads to minimum generated jitter.

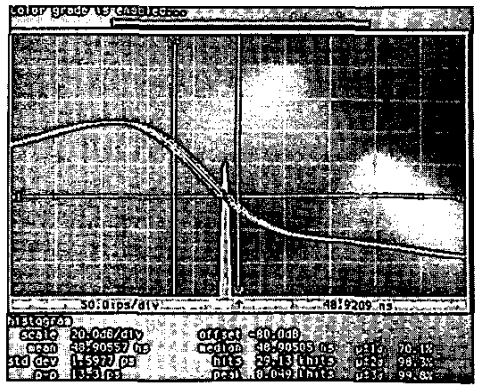

Figure 6. Clock jitter on a recurring pattern

In the case of the lower synchronization range circuit, and with a PRBS31 pattern is set at the input, the output clock jitter is 11 ps rms (Fig. 7).

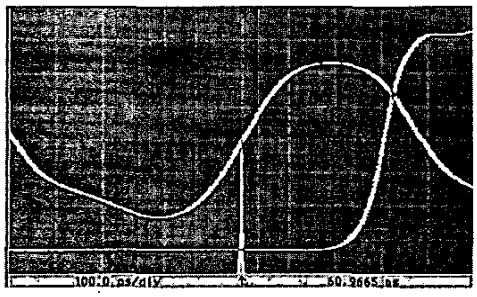

Figure 7. Clock jitter of prototype 1

On the second prototype (600 MHz of synchronization range), a PBRS31 pattern generates 40 ps rms and 26 ps rms jitter respectively on the output clock and the regenerated data (Fig. 8).

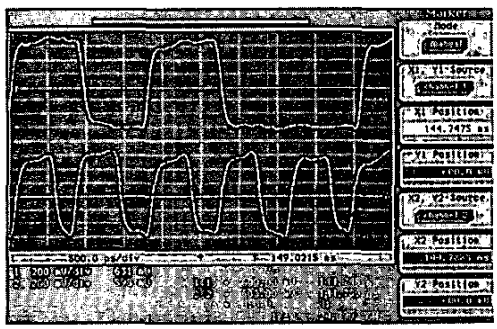

Figure 8. Recovered clock and data for PRBS31

The experimental results show us that in order to provide low jitter capability at the output regenerated data and clock, a rather low synchronization range is mandatory. This is mainly due to the ability of the injection-locked oscillator to be synchronized on harmonics on its input frequency. In case of random input signal (which can generated a numerous of harmonics), and if the SO has a large synchronization range, it will be locked on these parasitic references.

Moreover, the system is synchronized in less than one pattern, which is an inherent property of the SO, due to its large synchronization bandwidth. This is a major improvement versus classical CDR using DLL or PLL.

The main features of this chip are summarized in Table 1.

Table 1. Measurement results

Supply voltage	1.8 V
Power dissipation	300 mW (including 50 Ω buffers)
Free running frequency	1.09 GHz
Synchronization range	200 / 600 MHz
PRBS7 rms jitter	9.8 / 30 ps
PRBS31 rms jitter	11 / 40 ps
Technology	CMOS 6M1P 0.18 µm

VI. Conclusion

In this paper, we have presented a novel topology of open-loop CDR, which eradicates the major problem of these structures: the external components needed for the high-Q filters. The theoretical approach allows us an easy way to design a robust system whatever the process deviations. Moreover, compared with closed-loop structure, it drastically minimizes power consumption, size area, acquisition time (due to its inherent large synchronization range) and complexity. It is then well suited to be integrated in high-speed data link receivers.

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